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Please find below a communication from the EXAMINER in charge of this application.

Commissioner of Patents and Trademarks

Responsive to Communication Filed 7/5/01 .

The enclosed is a correct copy of a reference relating to the last Office action. The correction is indicated below.

THE PERIOD FOR RESPONSE OF 3 MONTHS SET IN SAID OFFICE ACTION IS RESTARTED TO BEGIN WITH THE DATE OF THIS LETTER.

☒ Part 1 - Correct Reference Citation

3,980,959 (George) 5,570,306 (Soo)

5,982,781 (Przybyla)

by Vivek Srivastava.
*Examiner*

☐ Part 2 - Correct Reference Furnished:

by _____
*Reference Order Center*

VIVEK SRIVASTAVA
PATENT EXAMINER

enc.

PTOL-316 (rev. 6/78)

## DETAILED ACTION

### *Claim Rejections - 35 U.S.C. § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, and 4 - 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background in view of George (3,980,959).

Regarding claim 1, Applicant's background discloses a video data transfer system (page 1 lines 8 - 10), a real time output path (page 1 lines 22 - 25, fig 3 item 25) through which video data processed by a video processor (fig 3 item 21) is sent to a display (fig 3 item 16) via a frame buffer (fig 3 item 14), a capturing-only path (page 2 lines 1 - 6 21 - 38, fig 3 item 27) which is independent of real time output path (fig 3 - capture-only path 27 to FIFO memory 24 and system memory 18 via system bus 17 is separate from real time output path 25 to display 16 via display control circuit 22) and through which video data is sent to a system memory via a system bus (page 2 lines 1- 6, fig 3 items 17 and 18).

The conventional video data transfer system in Applicant's background fails to disclose the claimed gate in the capturing only-path. A patent issued to George teaches a television

receiver comprising two terminals and a gate wherein the gate can be enabled or disabled thereby permitting or preventing signal flow between the terminals (see col 2 lines 46 - 57). It would have been obvious modifying the conventional video transfer system in Applicant's background to include a controllable gate enabling passing or blocking of video data would have prevented the passing of unwanted video data between the video processor and system memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the conventional video transfer system in Applicant's background to include the claimed gate to ensure the passing of data between the video processor and system memory only when required.

Considering claim 2, the conventional video transfer system in Applicant's background discloses a real time output path (fig 3 items 21, 14, 25, 16, page 1 lines 19 - 24), a capturing only path which is independent of the real time output path (fig 3 items 27, 17, 18, page 2 lines 1- 6, capturing only path 27 is independent from realtime output path 25), a real time output path comprising an offscreen memory which receives video data from video processor via a data bus and stored video data therein, the offscreen memory being in the frame buffer (fig 3 items 25, 14, 21, 13, 15 page 1 lines 19 - 24), a display control circuit which receives video data f rom the off-screen memory via the data bus for enlargement and interpolation processing and transfers results to the display (page 1 lines 8 - 24, fig 3 items 22, 13, 25, 16), and a capturing-only path which comprises a memory means for storing video data for transferring the video data to the system bus (page 2 lines 1 - 6, fig 3 items 24, 17, and 18).

The conventional video data transfer system in Applicant's background fails to disclose the claimed gate in the capturing only-path. A patent issued to George teaches a television receiver comprising two terminals and a gate wherein the gate can be enabled or disabled thereby permitting or preventing signal flow between the terminals (see col 2 lines 46 - 57). It would have been obvious modifying the conventional video transfer system in Applicant's background to include a controllable gate enabling passing or blocking of video data would have prevented the passing of unwanted video data between the video processor and system memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the conventional video transfer system in Applicant's background to include the claimed gate to ensure the passing of data between the video processor and system memory only when required.

Considering claim 4, the conventional video transfer system in Applicant's background discloses a capture path memory in a capture-only path (fig 3 item 24). The Applicant's background fails to disclose a capture path memory being connected to a gate and capture path memory being operable to store the video data passed by the gate. As discussed in claim 1, it would have been obvious to include a gate to ensure passing of data between the video processor and system only when required thus preventing unwanted data from reaching the system memory. It would have been obvious connecting the gate as claimed would have ensured passing data to the system memory only when required thus preventing unwanted data from being stored in the capture only path memory.

Considering claim 5, the conventional video transfer system in Applicant's background discloses wherein capture path memory is further effective to transfer the video data to system bus (page 2 lines 1 - 5, fig 3 item 24 and 17).

Considering claim 6, the conventional video transfer system in Applicant's background discloses wherein real time output path comprises an off-screen memory effective to receive video data from the video processor via a data bus and stores video data therein (fig 3 - off-screen memory 15 receives video data from video processor 21 via a data bus 13) and offscreen memory being in frame buffer (fig 3 items 14 and 15).

Considering claim 7, the conventional video transfer system in Applicant's background discloses providing video data from video processor to a plurality of paths independent of each other (fig 3 data from video processor is provided to frame buffer data bus path 13 and capture only path 27 and real time output path 25), sending video data to a display through a frame buffer in at least one of independent paths operating as a real time output path (fig 3 - data is sent through frame buffer 14 to display 16 via independent real time output path 25, page 1 lines 19 - 24), sending video data to a system memory through a system bus in at least another of independent paths operating as a capture-only path (fig 3 items 27, 24, 17 and 18, page 2 lines 1 - 6).

The conventional video transfer system in Applicant's background fails to disclose controlling capture-only path to permit video data to pass to system memory when video data is to be captured. A patent issued to George teaches a television receiver comprising two terminals

and a gate wherein the gate can be enabled or disabled thereby permitting or preventing signal flow between the terminals (see col 2 lines 46 - 57). It would have been obvious modifying the conventional video transfer system in Applicant's background to include a controllable gate would have enabled controlling the capture-only path for passing or blocking of video data between the video processor and system memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the conventional video transfer system in Applicant's background to include the claimed controlling the capture-only path to ensure the passing of data between the video processor and system memory only when required.

Considering claim 8, the conventional video transfer system in Applicant's background discloses storing video data in a capture only path memory in capture-only path when video data is permitted to pass to system memory (page 2 lines 1 - 6 and fig 3 items 24, 17, and 18, if data is passed to memory 18 it must first be saved in FIFO 24).

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background in view of George (3,980,959), as applied to claim 2 above, and further in view of Przybyla et al (5,982781) and Soo (5,570,306).

Considering claim 3, the combination of the Applicant's background and George fails to disclose wherein the memory means transfers stored video data to the system bus when system bus is not occupied by some other unit and when system bus is occupied by some other unit,

checks if stored data contains a field delimiter or a frame delimiter and closes said gate to stop data transfer when stored data contains the delimiter and, when the stored data does not contain the delimiter, stores the next video data passing through the gate.

Przybyla teaches by checking if a bus is occupied or not before data transmission, loss of data and re-transmission of data is avoided. It would have been obvious to modify the combination of the Applicant's background and George to check to see if the system bus is occupied by other devices to prevent loss of data or re-transmission of data. Soo teaches a frame delimiter can be used to indicate a buffer overflow condition (col 11 lines 1- 10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of the Applicant's background and George based on the teachings of Przybyla and Soo to include checking of the system bus as claimed and to include checking the video data stored in the capture path memory for a frame delimiter to ensure data is not lost or would need re-transmission and to prevent an overflow condition in the capture path memory.

4. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background in view of George (3,980,959), as applied to claim 8 above, and further in view of Przybyla et al (5,982781).

Considering claim 9, the Applicant's background and George fail to disclose checking system bus for occupation by other devices connected thereto.

Przybyla teaches by checking if a bus is occupied or not before data transmission, loss of data and re-transmission of data is avoided. It would have been obvious to modify the combination of the Applicant's background and George to check to see if the system bus is occupied by other devices to prevent loss of data or re-transmission of data. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of the Applicant's background and George based on the teachings of Przybyla to include checking of the system bus as claimed to ensure data is not lost or would need re-transmission.

Regarding claim 10, the combination of Applicant's background and George fails to disclose the claimed transferring video data from capture path memory to system memory when system bus is not occupied by other devices connected thereto.

It would have been obvious from the teaches of Pryzbyla, as discussed in claim 9, checking to see if the system bus is not occupied by another device before transferring data would have avoided data loss and the need for re-transmitting data. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Applicant's background and George to include transferring video data from capture path memory to system memory when system bus is not occupied by other devices connected thereto to avoid data loss and the need for re-transmission.

5. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background in view of George (3,980,959), and further in view of Przybyla et al (5,982781) as applied to claim 10 above, and further in view of Soo (5,570,306).

The combination of Applicant's background, George and Pryzbyla fail to disclose checking video data stored in the capture path memory for at least one of a field and a frame delimiter when the system bus is occupied. Soo teaches a frame delimiter can be used to indicate a buffer overflow condition (col 11 lines 1 - 10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of the Applicant's background, George and Pryzbyla to include checking the video data stored in the capture path memory for a frame delimiter to prevent an overflow condition in the capture path memory.

Regarding claim 12, the combination of the Applicant's background, George and Pryzbyla fail to disclose controlling capture-only path to prevent video data from being stored in the capture path memory when the capture path memory contains a frame delimiter.

As discussed in claim 11, from the teachings of Pryzbyla, it would have been obvious to include checking for a frame delimiter to prevent an overflow condition in the capture path memory. It would have been obvious to control the capture-only path to prevent video data from being stored in the capture-only path memory when the capture-only path memory contains a frame delimiter to prevent further overflow of the capture only path memory.

*Allowable Subject Matter*

6. The indicated allowability of claims 2 and 3 is withdrawn in view of the newly discovered reference(s) to the Applicant's background. Rejections based on the newly cited reference(s) follow.

*Response to Arguments*

7. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

*Conclusion*

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reddy (6,081,279) - Shared memory graphics accelerator system

Storm et al (5,999,196) - Processing units for graphics accelerator

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(703) 308-9051, (for formal communications intended for entry)

**Or:**

(703) 308- 5359 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vivek Srivastava whose telephone number is (703) 305 - 4038. The examiner can normally be reached on Monday - Thursday from 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andy Faile, can be reached at (703) 305 - 4380.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 305 - 3900.

VS 6/29/01

VIVEK SRIVASTAVA
PATENT EXAMINER